HAREM: High Aspect Ratio Etching and Metallization

HAREM 高アスペクト比シリコンマイクロマシニング加工法

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We report a novel bulk micromachining method for the fabrication of high aspect ratio monocrystalline silicon MEMS in a standard silicon wafer. The two-mask method combines double-side etching and metallization to create a micromechanical device with 'insulating walls' on its backside. The insulating walls ensure a proper electrical insulation between different actuation and sensing elements situated on either fixed or movable parts of the device. To demonstrate the many potential applications of this simple microfabrication method, we have machined and characterized electrostatically-actuated microtweezers with an integrated differential capacitive sensor.

Keywords: HAREM, DRIE etching, DNA tweezers, Differential Capacitive sensor.

1. INTRODUCTION

In most cases, MEMS devices require effective electrical insulation between the mechanically linked microstructures. Vertical trench isolation technology, based on either SOI [1] or standard silicon substrates [2], employs etched trenches refilled with a dielectric material to create distinct electrical domains on both fixed and movable structures, allowing for a wide range of design possibilities. However, in order to ensure reliable electrical isolation and mechanical integrity, strict requirements are imposed on etching and refilling of the trenches, making the process rather complicated.

Here, we present a new and sophisticated bulk micromachining method for creating electrically isolated areas without using refilled trenches. We call this method High Aspect Ratio Etching and Metallization, or HAREM. Compared to the well-known SCREAM process [3], which is also based on etching and metallization, the HAREM process additionally offers (i) the possibility to define distinct electrical domains on movable parts, (ii) a non-critical release of microstructures, and (iii) a simplified mask design, all at the sole cost of an additional lithography mask.

2. HAREM FABRICATION PROCESS

The two-mask process is illustrated in Fig. 1. Starting from a standard silicon wafer (1), insulating walls are etched and partly undercut by the combination of anisotropic and isotropic plasma etching (2). On the opposite side, the microsystem is etched and directly released by deep RIE (3). After passivation (4), actuation and sensing electrodes are formed by metal sputtering (5). The shape of the insulating walls ensures proper electrical insulation between the electrodes. Depending on the application, the insulating walls can be configured in many different ways. Fig. 2 shows three basic configurations.

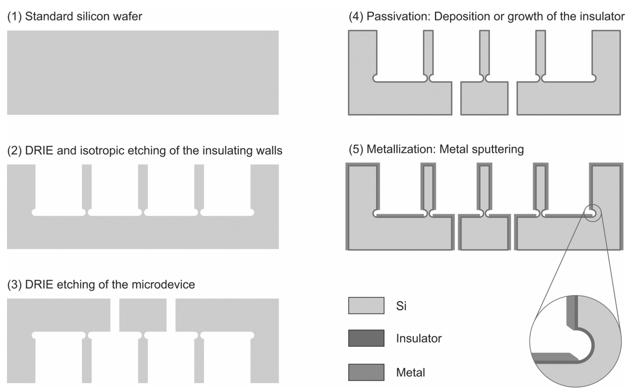

***Figure 1** HAREM microfabrication flow process. In this work, we employed thermal oxidation for passivation and aluminum sputtering for metallization.*

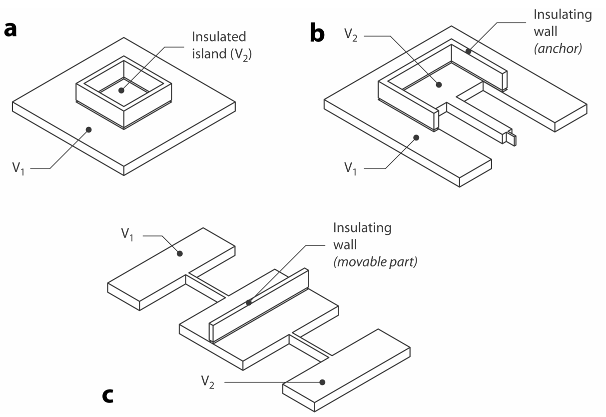

Figure 2 *Typical cases showing the potential of HAREM technology.* ***a)*** *Electrically insulated "island" structure supported by the silicon substrate.* ***b)*** *A fixed probe which is electrically insulated from the handling substrate.*
c) *Two movable and mechanically anchored elements which are electrically insulated.* V_1 *and* V_2 *refer to the electrical potentials of the structures separated by an insulating wall.*

3. RESULTS

In order to demonstrate the feasibility and the design possibilities of the HAREM process, we have fabricated a micromanipulator for biophysical experimentation based on our previously realized prototype made with an adapted SOI micromachining process [4]. SEM pictures of the device are shown in Fig. 3. The device consists of an electrostatic comb-drive actuator for displacement of the tweezers and an integrated differential capacitance used for the sensing of relative position (Fig. 3, *left*). Fig. 3 (*center*) shows the 'insulating side' of the device with insulating walls situated on both fixed and movable parts. In total, six different electrical zones were created: two for the actuator (P_1, P_2), three for the differential capacitive sensor (P_3, P_4, P_5) and one for the moving probe (P_6).

After fabrication, the silicon chip was mounted and wire-bonded on a PCB (Fig. 3, *right*). The prototype showed an electrical insulation better than 1 GΩ between the different elements of the device. Furthermore, using the differential capacitive sensor and a lock-in amplifier circuit [5], we could measure the relative displacement of the tweezers with few nanometers resolution for a displacement range of around 3 µm (Fig. 4).

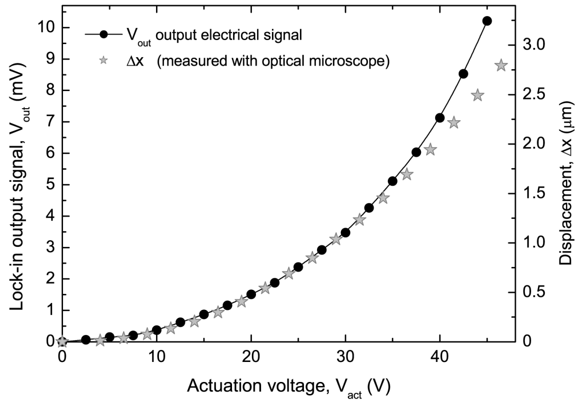

Figure 4 *Electrical signal of the capacitive sensor (•) as compared to the displacement measured by optical method (★).*

4. CONCLUSION

A bulk micromachining technology for the fabrication of high aspect ratio monocrystalline microstructures in a standard silicon wafer is presented. Sophisticated electrical insulation, low-cost of the starting substrate and large design flexibility make this technology highly suitable for diverse MEMS applications.

References

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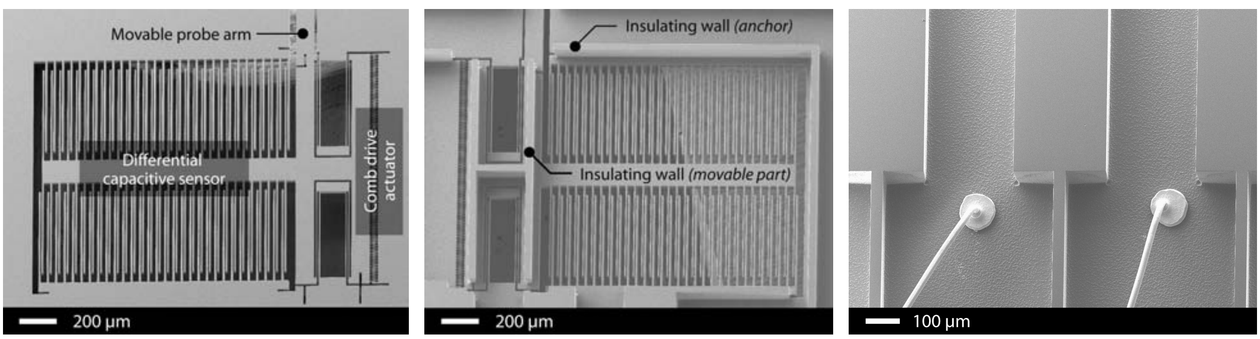

Figure 3 *SEM pictures of the microtweezers: (left) 'device side', (center) 'insulating side', and (right) wire bonding on the 'insulating side'. The thickness of the structure is 60 µm. Insulating walls are 140 µm high, 40 µm wide, with 2 µm undercut. The smallest elements are 3 µm wide (fingers of the comb-drive).*